ISO9001:2000 Certified SCI Quality System

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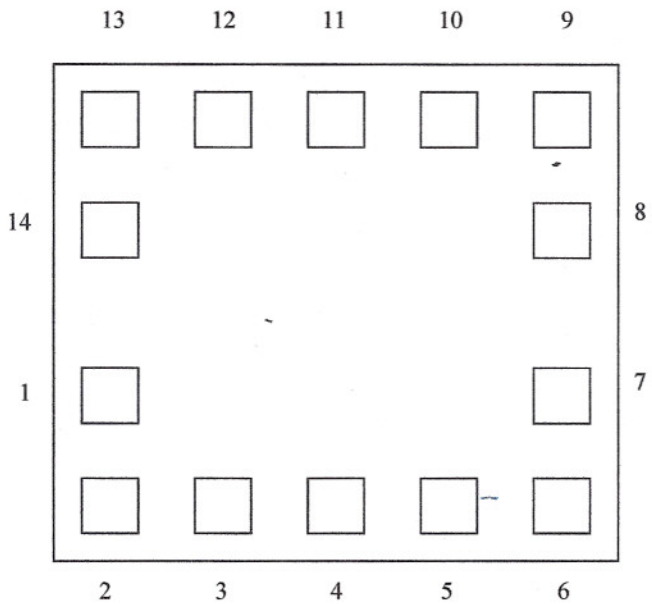
PAD FUNCTION



The information for this layout is believed to be correct at the time of issue.
Please verify your requirements prior to commencement of any assembly process, as no liability for omission or error can be accepted.
All devices supplied against this padlayout will comply with the physical dimensions shown, to a tolerance of ± 3 mils.
Chip back potential is the level at which bulk silicon is maintained either by bond pad connection or in some cases the potential to which the chip back must be connected if stated above.
Pad positions shall obey the following rules:

1. Pad functions shall not change sequence and shall agree with the above definitions.
2. No pad function shall move by more than 1mm from the position shown.
3. No pad function shall move from a corner, and another move into that corner, even if the above constraints are met.

Note: 1 mil = 0.001 inch

APPROVED	54LS32	DIE INFORMATION
IAN HARVEY ..... DATE: 16/8/1985	NATIONAL SEMICONDUCTOR	DIMENSIONS (Mils): 37 x 32 BOND PADS: MASK. REF: GEOMETRY: BACK POTENTIAL:
SERIAL/ISSUE NO. 003874		METALLISATION/THICKNESS (KA) TOP: BACK: